WHAT IS CLAIMED IS:

Sub a3

1. A module comprising:

a semiconductor device;

a phase adjustment circuit generating a second clock so that a phase adjustment signal output from the semiconductor device and a first clock have a predetermined phase relationship; and

an output circuit that is provided in the semiconductor device and generates the phase adjustment signal from the second clock.

2. The module as claimed in claim 1, wherein the semiconductor device comprises an output buffer from which data is output in synchronism with the second clock.

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3. A module comprising:

semiconductor devices;

a phase adjustment circuit generating a second clock so that a phase adjustment signal output from a first semiconductor device that is one of the semiconductor devices and a first clock have a predetermined phase relationship, the second clock being supplied to the semiconductor devices; and

a wiring board on which the semiconductor devices and the phase adjustment circuit are mounted,

the first semiconductor device including

Sub a4 an output circuit generating the phase adjustment signal from the second clock.

4. The module as claimed in claim 3, wherein each of the semiconductor devices comprises an output buffer from which data is output in synchronism with the second clock.

5. The module as claimed in claim 3, wherein the module comprises first data lines over which data output from the semiconductor devices are transferred, and a second data line over which the phase adjustment signal output from the first semiconductor device is transferred,

the first and second data lines being provided on the wiring board.

6. The module as claimed in claim 4, wherein the module comprises first data lines over which data output from the semiconductor devices are transferred, and a second data line over which the phase adjustment signal output from the first semiconductor device is transferred,

the first and second data lines being provided on the wiring board.

7. The module as claimed in claim 5, wherein the first and second data lines are arranged on an identical side of the wiring board.

8. The module as claimed in claim 6, wherein the first and second data lines are arranged on an identical side of the wiring board.

9. The module as claimed in claim 5, wherein the first and second data lines are arranged on opposite sides of the wiring board so that the semiconductor devices are sandwiched between the first and second data lines.

10. The module as claimed in claim 6, wherein the first and second data lines are arranged on opposite sides of the wiring board so that the semiconductor devices are sandwiched between the first and second data lines.

11. The module as claimed in claim 5, wherein the first and second data lines have a substantially identical delay amount.

12. The module as claimed in claim 6, wherein the first and second data lines have a substantially identical delay amount.

13. The module as claimed in claim 5, wherein the first and second data lines have a length that allows their delay amounts to be negligible.

14. The module as claimed in claim 6, wherein the first and second data lines have a length that allows their delay amounts to be negligible.

15. The module as claimed in claim 3, further comprising a terminal that is provided on the wiring board and is used to output the phase adjustment signal to an outside of the module.

16. The module as claimed in claim 3, wherein the first semiconductor device generates the phase adjustment signal in accordance with a predetermined signal given from an outside of the first semiconductor device.

17. The module as claimed in claim 3, wherein:

the semiconductor devices including the first semiconductor device have an identical circuit configuration; and

the first semiconductor device has an output circuit that receives an external instruction that instructs the first semiconductor device to generate the phase adjustment signal.

18. The module as claimed in claim 3, wherein the first clock is supplied from an outside of the module.

19. The module as claimed in claim 3, further comprising a circuit generating the first clock from an external clock.

20. The module as claimed in claim 3, wherein each of the semiconductor devices comprises a programmable delay circuit that delays the second clock.

21. The module as claimed in claim 3, wherein the semiconductor devices comprise semiconductor memory devices.

22. The module as claimed in claim 3, wherein the phase adjustment circuit generates the second clock from dummy output data output by the first semiconductor device.

23. The module as claimed in claim 3, further comprising a second phase adjustment circuit generating a third clock so that the third clock and the first clock have a predetermined phase relationship, the third clock being supplied to the semiconductor devices.

24. The module as claimed in claim 23, wherein the first clock corresponds to the third clock.

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25. A system comprising:

~~modules;~~

a wiring board ~~on~~ which the modules are mounted; and

a dummy output load line ~~serving as~~ loads of dummy output data output from the modules.

26. The system as claimed in claim 25, wherein the dummy output load line is provided in common to the modules.

27. The system as claimed in claim 25, wherein the dummy output load line comprises parts respectively provided to the modules.

28. The system as claimed in claim 25, wherein the modules comprises a module including:

semiconductor devices;

a phase adjustment circuit generating a second clock so that a phase adjustment signal output from a first semiconductor device that is one of the semiconductor devices and a first clock have a predetermined phase relationship, the second clock being supplied to the semiconductor devices; and

a wiring board on which the semiconductor devices and the phase adjustment circuit are mounted,

the first semiconductor device including an output circuit generating the phase adjustment signal from the second clock.

29. A semiconductor device comprising:

a first buffer receiving a first external clock and generating a first internal clock therefrom;

a second buffer receiving a second external clock and generating a second internal clock therefrom;

an input buffer fetching input data in synchronism with the first internal clock;

an output buffer from which data is output in synchronism with the second internal clock; and

an output circuit outputting dummy output

data in synchronism with the second internal clock.

30. The semiconductor device as claimed in claim 29, wherein the output circuit generates the dummy output data from the second internal clock in accordance with an instruction to output the dummy output data supplied from an outside of the semiconductor device.

31. The semiconductor device as claimed in claim 29, wherein the output circuit comprises a programmable delay circuit that delays the second internal clock.

32. The semiconductor device as claimed in claim 30, wherein the output circuit comprises a programmable delay circuit that delays the second internal clock.

33. The semiconductor device as claimed in claim 29, wherein the semiconductor device is a semiconductor memory device.